MEMORY SYSTEM WITH DYNAMIC TIMING CORRECTION

ABSTRACT OF THE DISCLOSURE

A memory system includes a memory controller and a bank of memory devices. The memory controller controls the memory devices through packets of control data and a master clock signal. Each of the memory devices includes an adjustable output timing vernier that can be adjusted in response to commands from the memory controller. The vernier output controls timing of output data relative to the master clock signal. As each memory device transmits data to the memory controller, the memory device also transmits an echo clock signal coincident with the data. The memory controller receives the echo clock signal and compares the echo clock signal to the master clock signal to identify shifts in timing of the echo clock signal. If the echo clock signal shifts by more than one vernier increment from the master clock signal, the master controller issues a command to the memory device to adjust the output vernier to correct the timing drift of the echo clock signal. By correcting the timing drift of the echo clock signal, the memory controller also corrects timing drift of the output data, thereby assuring that the data arrive at the memory controller coincident with edges of the master clock signal.